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Processor Architecture From Dataflow To Superscalar And Beyond

4. ARM core Dataflow Model |ARM 7 | LPC2148 | Advanced Processors Architecture All Access: Modern CPU Architecture Part 1 – Key Concepts | Intel Technology Rethinking Processor and System Architecture How a CPU Works in 100 Seconds // Apple Silicon M1 vs Intel i9 PA 6.4 ARM Data-flow Model with Example Dataflow engines: an increasingly mainstream computer architecture 4.5 Data flow architecture David Patterson: Computer Architecture and Data Storage | Lex Fridman Podcast #104 L-1.2: Von Neumann's Architecture | Stored Memory Concept in Computer Architecture Stanford Seminar - Dataflow for convergence of AI and HPC - GroqChip! Data Flow Diagram EXAMPLE [How to Create Data Flow Diagrams] CPU Architecture Dataflow Computing for Data-intensive Applications Digital Design \u0026 Comp. Arch. - Lecture 16a: Dataflow \u0026 Superscalar Exec. (ETH Zürich, Spring 2020) Architecture All Access: Modern CPU Architecture 2 - Microarchitecture Deep Dive | Intel Technology The Mill CPU Architecture - Execution (6 of 13) What is CPU Architecture? An intuitive approach for understanding the CPU and RAM
Advanced Topics in Dataflow Computing and Multithreading
Hardware/Software Co-Design for Data Flow Dominated Embedded Systems
Implementation of a General-purpose Dataflow Multiprocessor
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Algorithms and Architectures for Real-Time Control 1992
A Computer Architecture for Data-flow Computation
Multiple Input Node Dataflow Processor Architecture

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Advanced Topics in Dataflow Computing and Multithreading Springer Science & Business Media
Abstract: "An efficient static dataflow architecture based on an argument-fetching data-driven principle has recently been proposed (as reported by Dennis and Gao [5]). This architecture opens possibilities in combining the techniques of existing high-performance conventional pipelined architectures with the strengths of the dataflow model of parallel computation. The key feature is that data never 'flows' in the new architecture even though instruction scheduling remains data-driven. The new architecture answers some speculations about the efficiency of practical dataflow architectures -- data-driven instruction scheduling need not mean higher traffic due to data token flow in the processor architecture.
Hardware/Software Co-Design for Data Flow Dominated Embedded Systems Jones & Bartlett Learning
This book gathers the refereed proceedings of the Applied Informatics and Cybernetics in Intelligent Systems Section of the 9th Computer Science On-line Conference 2020 (CSOC 2020), held on-line in April 2020. Modern cybernetics and computer engineering in connection with intelligent systems are an essential aspect of ongoing research. This book addresses these topics, together with automation and control theory, cybernetic applications, and the latest research trends.
Implementation of a General-purpose Dataflow Multiprocessor Wiley-IEEE Computer Society Press
This useful text/reference describes the implementation of a varied selection of algorithms in the DataFlow paradigm, highlighting the exciting potential of DataFlow computing for applications in such areas as image understanding, biomedicine, physics simulation, and business. The mapping of additional algorithms onto the DataFlow architecture is also covered in the following Springer titles from the same team: DataFlow Supercomputing Essentials: Research, Development and Education, DataFlow Supercomputing Essentials: Algorithms, Applications and Implementations, and Guide to DataFlow Supercomputing. Topics and Features: introduces a novel method of graph partitioning for large graphs involving the construction of a skeleton graph; describes a cloud-supported web-based integrated development environment that can develop and run programs without DataFlow hardware owned by the user; showcases a new approach for the calculation of the extrema of functions in one dimension, by implementing the Golden Section Search algorithm; reviews algorithms for a DataFlow architecture that uses matrices and vectors as the underlying data structure; presents an algorithm for spherical code design, based on the variable repulsion force method; discusses the implementation of a face recognition application, using the DataFlow paradigm; proposes a method for region of interest-based image segmentation of mammogram images on high-performance reconfigurable DataFlow computers; surveys a diverse range of DataFlow applications in physics simulations, and investigates a DataFlow implementation of a Bitcoin mining algorithm. This unique volume will prove a valuable reference for researchers and programmers of DataFlow computing, and supercomputing in general. Graduate and advanced undergraduate students will also find that the book serves as an ideal supplementary text for courses on Data Mining, Microprocessor Systems, and VLSI Systems.
Creativity in Computing and DataFlow SuperComputing Springer
Future computing professionals must become familiar with historical computer architectures because many of the same or similar techniques are still being used and may persist well into the future. Computer Architecture: Fundamentals and Principles of Computer Design discusses the fundamental principles of computer design and performance enhancement that have proven effective and demonstrates how current trends in architecture and implementation rely on these principles while expanding upon them or applying them in new ways. Rather than focusing on a particular type of machine, this textbook explains concepts and techniques via examples drawn from various architectures and implementations. When necessary, the author creates simplified examples that clearly explain architectural and implementation features used across many computing platforms. Following an introduction that discusses the difference between architecture and implementation and how they relate, the next four chapters cover the architecture of traditional, single-processor systems that are still, after 60 years, the most widely used computing machines. The final two chapters explore approaches to adopt when single-processor systems do not reach desired levels of performance or are not suited for intended applications. Topics include parallel systems, major classifications of architectures, and characteristics of unconventional systems of the past, present, and future. This textbook provides students with a thorough grounding in what constitutes high performance and how to measure it, as well as a full familiarity in the fundamentals needed to make systems perform better. This knowledge enables them to understand and evaluate the many new systems they will encounter throughout their professional careers.
Polymorphic Computing Architecture Based on a Dataflow Processor Core Springer Nature
Expert systems and real-time systems technology have been developed independently. Expert systems have been successfully implemented in many complex applications traditionally performed by human experts. Real-time systems have been successfully applied in areas requiring interaction with dynamic environments, control and monitoring applications for example. Merging these two technologies will yield intelligent systems capable of interacting with complex dynamic environments, an area in which human operators exhibit poor productivity, due to cognitive overload.
Academic Press
This thesis research is a study of a novel processor architecture for a massively parallel computer system. An existing simulation of the Fresh Breeze architecture has been extended to incorporate a multi-level memory hierarchy and dynamic load balancing. An efficient hardware-based garbage collection mechanism has been proposed. Various design trade-offs are evaluated. The simulation demonstrates that the architecture can support memory access with DRAM latency and still achieve high processor utilization.
Computer Architecture Springer Science & Business Media
Implementation of a General Purpose Dataflow Multiprocessor extends work in this area by introducing an unusually simple model of dynamic dataflow execution, called the Explicit Token Store (ETS) architecture, and its realization in Monsoon, a large-scale dataflow multiprocessor.
Computer Architecture Technology Trends Gulf Professional Publishing
The book includes papers on massively parallel distributed memory and multithreaded architecture design, synchronization and pipelined design, and superpipelined data-driven VLSI processors. Other sections discuss stream data types, the development of well-structured software, and parallelization of dataflow programs.
Real-Time Expert Systems Computer Architecture IEEE Computer Society
The book presents a succession of RISC-V processor implementations in increasing difficulty (non pipelined, pipelined, deeply pipelined, multithreaded, multicore). Each implementation is shown as an HLS (High Level Synthesis) code in C++ which can really be synthesized and tested on an FPGA based development board (such a board can be freely obtained from the Xilinx University Program targeting the university professors). The book can be useful for three reasons. First, it is a novel way to introduce computer architecture. The codes given can serve as labs for a processor architecture course. Second, the book content is based on the RISC-V Instruction Set Architecture,

which is an open-source machine language promised to become the machine language to be taught, replacing DLX and MIPS. Third, all the designs are implemented through the High Level Synthesis, a tool which is able to translate a C program into an IP (Intellectual Property). Hence, the book can serve to engineers willing to implement processors on FPGA and to researchers willing to develop RISC-V based hardware simulators.

DataFlow Supercomputing Essentials

Morgan Kaufmann
The Fifth Generation Computer Project is a two-part book consisting of the invited papers and the analysis. The invited papers examine various aspects of The Fifth Generation Computer Project. The analysis part assesses the major advances of the Fifth Generation Computer Project and provides a balanced analysis of the state of the art in The Fifth Generation. This part provides a balanced and comprehensive view of the development in Fifth Generation Computer technology. The Bibliography compiles the most important published material on the subject of The Fifth Generation.
Advanced Topics in Dataflow Computing and Multithreading Waveland Press
Essentials of Computer Organization and Architecture focuses on the function and design of the various components necessary to process information digitally. This title presents computing systems as a series of layers, taking a bottom–up approach by starting with low-level hardware and progressing to higher-level software. Its focus on real-world examples and practical applications encourages students to develop a “big-picture” understanding of how essential organization and architecture concepts are applied in the computing world. In addition to direct correlation with the ACM/IEEE guidelines for computer organization and architecture, the text exposes readers to the inner workings of a modern digital computer through an integrated presentation of fundamental concepts and principles.
A preliminary architecture for a basic data flow processor CRC Press
Conceptual and precise, Modern Processor Design brings together numerous microarchitectural techniques in a clear, understandable framework that is easily accessible to both graduate and undergraduate students. Complex practices are distilled into foundational principles to reveal the authors insights and hands-on experience in the effective design of contemporary high-performance micro-processors for mobile, desktop, and server markets. Key theoretical and foundational principles are presented in a systematic way to ensure comprehension of important implementation issues. The text presents fundamental concepts and foundational techniques such as processor design, pipelined processors, memory and I/O systems, and especially superscalar organization and implementations. Two case studies and an extensive survey of actual commercial superscalar processors reveal real-world developments in processor design and performance. A thorough overview of advanced instruction flow techniques, including developments in advanced branch predictors, is incorporated. Each chapter concludes with homework problems that will institute the groundwork for emerging techniques in the field and an introduction to multiprocessor systems.
Parallel and Distributed Processing and Applications Cambridge, Mass. : MIT Press
This book constitutes the thoroughly refereed post-conference proceedings of the 5th International ICST Conference on Bio-Inspired Models of Network, Information, and Computing Systems (BIONETICS 2010) which was held in Boston, USA, in December 2010. The 78 revised full papers were carefully reviewed and selected from numerous submissions for inclusion in the proceedings. BIONETICS 2010 aimed to provide the understanding of the fundamental principles and design strategies in biological systems and leverage those understandings to build bio-inspired systems.
Network Processors Elsevier
As the demand for digital communication networks has increased, so have the challenges in network component design. To meet ever-escalating performance, flexibility, and economy requirements, the networking industry has opted to build products around network processors. These new chips range from task-specific processors, such as classification and encryption engines, to more general-purpose packet or communications processors. Programmable yet application-specific, their designs are tailored to efficiently implement communications applications such as routing, protocol analysis, voice and data convergence, firewalls, VPNs, and QoS. Network processor design is an emerging field with issues and opportunities both numerous and formidable. To help meet this challenge, the editors of this volume created the first Workshop on Network Processors, a forum for scientists and engineers from academia and industry to discuss their latest research in the architecture, design, programming, and use of these devices. In addition to including the results of the Workshop in this volume, the editors also present specially commissioned material from practicing designers, who discuss their companies' latest network processors. Network Processor Design: Issues and Practices is an essential reference on network processors for graduate students, researchers, and practicing designers. * Includes contributions from major academic and industrial research labs including Aachen University of Technology; Cisco Systems; Infineon Technologies; Intel Corp.; North Carolina State University; Swiss Federal Institute of Technology; University of California, Berkeley; University of Dortmund; University of Washington; and Washington University. * Examines the latest network processors from Agere Systems, Cisco, IBM, Intel, Motorola, Sierra Inc., and TranSwitch.
Algorithms and Architectures for Real-Time Control 1992 John Wiley & Sons
A Multi-Processor System-on-Chip (MPSoC) is the key component for complex applications. These applications put huge pressure on memory, communication devices and computing units. This book, presented in two volumes – Architectures and Applications – therefore celebrates the 20th anniversary of MPSoC, an interdisciplinary forum that focuses on multi-core and multi-processor hardware and software systems. It is this interdisciplinarity which has led to MPSoC bringing together experts in these fields from around the world, over the last two decades. Multi-Processor System-on-Chip 2 covers application-specific MPSoC design, including compilers and architecture exploration. This second volume describes optimization methods, tools to optimize and port specific applications on MPSoC architectures. Details on compilation, power consumption and wireless communication are also presented, as well as examples of modeling frameworks and CAD tools. Explanations of specific platforms for automotive and real-time computing are also included.
A Computer Architecture for Data-flow Computation Springer
A survey of architectural mechanisms and implementation techniques for exploiting fine- and coarse-grained parallelism within microprocessors. Beginning with a review of past techniques, the monograph provides a comprehensive account of state-of-the-art techniques used in microprocessors, covering both the concepts involved and implementations in sample processors. The whole is rounded off with a thorough review of the research techniques that will lead to future microprocessors. XXXXXXX Neuer Text This monograph surveys architectural mechanisms and implementation techniques for exploiting fine-grained and coarse-grained parallelism within microprocessors. It presents a comprehensive account of state-of-the-art techniques used in microprocessors that covers both the concepts involved and possible implementations. The authors also provide application-oriented methods and a thorough review of the research techniques that will lead to the development of future processors.
Multiple Input Node Dataflow Processor Architecture Springer Nature
This informative text/reference highlights the potential of DataFlow computing in research requiring high speeds, low power requirements, and high precision, while also benefiting from a reduction in the size of the equipment. The cutting-edge research and implementation case studies provided in this book will help the reader to develop their practical understanding of the advantages and unique features of this methodology. This work serves as a companion title to DataFlow Supercomputing Essentials: Algorithms, Applications and Implementations, which reviews the key algorithms in this area, and provides useful examples. Topics and features: reviews the library of tools, applications, and source code available to support DataFlow programming; discusses the enhancements to DataFlow computing yielded by small hardware changes, different compilation techniques, debugging, and optimizing tools; examines when a DataFlow architecture is best applied, and for which types of calculation; describes how converting applications to a DataFlow representation can result in an acceleration in performance, while reducing the power consumption; explains how to implement a DataFlow application on Maxeler hardware architecture, with links to a video tutorial series available online. This enlightening volume will be of great interest to all researchers investigating supercomputing in general, and DataFlow computing in particular. Advanced undergraduate and graduate students involved in courses on Data Mining, Microprocessor Systems, and VLSI Systems, will also find the book to be a helpful reference.
Guide to Computer Processor Architecture Elsevier
Processor ArchitectureSpringer Science & Business Media
The Fifth Generation Computer Project Elsevier
It is universally accepted today that parallel processing is here to stay but that software for parallel machines is still difficult to develop. However, there is little recognition of the fact that changes in processor architecture can significantly ease the development of software. In the seventies the availability of processors that could address a large name space directly, eliminated the problem of name management at one level and paved the way for the routine development of large programs. Similarly, today, processor architectures that can facilitate cheap synchronization and provide a global address space can simplify compiler development for parallel machines. If the cost of synchronization remains high, the pro gramming of parallel machines will remain significantly less abstract than programming sequential machines. In this monograph Bob Iannucci presents the design and analysis of an architecture that can be a better building block for parallel machines than any von Neumann processor. There is another very interesting motivation behind this work. It is rooted in the long and venerable history of dataflow graphs as a formalism for ex pressing parallel computation. The field has bloomed since 1974, when Dennis and Misunas proposed a truly novel architecture using dataflow graphs as the parallel machine language. The novelty and elegance of dataflow architectures has, however, also kept us from asking the real question: "What can dataflow architectures buy us that von Neumann ar chitectures can't?" In the following I explain in a round about way how Bob and I arrived at this question.
Applied Informatics and Cybernetics in Intelligent Systems Springer Science & Business Media
The 1992 Parallel Architectures and Languages Europe conference continues the tradition - of a wide and representative international meeting of specialists from academia and industry in theory, design, and application of parallel computer systems - set by the previous PARLE conferences held in Eindhoven in 1987, 1989, and 1991. This volume contains the 52 regular and 25 poster papers that were selected from 187 submitted papers for presentation and publication. In addition, five invited lectures areincluded. The regular papers are organized into sections on: implementation of parallel programs, graph theory, architecture, optimal algorithms, graph theory and performance, parallel software components, data base optimization and modeling, data parallelism, formal methods, systolic approach, functional programming, fine grain parallelism, Prolog, data flow systems, network efficiency, parallel algorithms, cache systems, implementation of parallel languages, parallel scheduling in data base systems, semantic models, parallel data base machines, and language semantics.