OMB No. 3329786528495

Dynamic Voltage Scaling And Power Management For Portable

Power Consumption | Dynamic Voltage and Frequency Scaling (DVFS) System Power Savings Using Dynamic Voltage Scaling Why DVFS? 2. Ultra Dynamic Voltage Scaling : Error Resiliency, Power dissipation and Reliability Mod-01 Lec-22 Supply Voltage Scaling - I Lecture 53 : Critical Performance Limits in Dynamic Voltage Scaling and Possible Solutions 3.11 Dynamic voltage and frequency scaling Adaptive voltage scaling for high-performance DSPs Dynamic Voltage Frequency Scaling Experiment 4 Dynamic Voltage Scaling Can you handle the truth about dynamic range compression? DVFS - Dynamic voltage and frequency scaling POWER GATING The Planck scale: Is there a fundamental limit to space and time? Applied Vibration Analysis: Analyzing Gear Vibrations Lecture 3: Passive Component Sizing Lesson 2: Scaling Waveforms Power Supplies - Isolated and Regulated Become An Electrical Lineworker Techniques to Reduce Power Noise

Margin, Trends, Power Consumption, Switching, Dynamic Voltage Scaling of Digital Systems What are the different types of power optimization? IQ TEST VLSI - UPF - Low-power Methodology, Design and Verification (Written Course) Preview Power and Reliability in Extreme Scale Computing 13 3 30pm Sub microsecond Adaptive Voltage Scaling in a 28nm RISC V SoC Ben Keller, UC Berkeley Just physics student things #shorts #math #astrophysics 3.6 Introduction to Supply voltage scaling for low power A satisfying chemical reaction ECE203 - Lecture 11 - Low-Power Digital Design

Controlling Energy Demand in Mobile Computing Systems

Dynamic Voltage Scaling with Feedback Scheduling for Real-time Embedded Systems

Multi-voltage CMOS Circuit Design

Power Aware Computing

Low-Power VLSI Circuits and Systems

Integrated Circuit and System Design: Power and Timing Modeling, Optimization and Simulation

Just-in-Time Dynamic Voltage Scaling: Exploiting Inter-Node Slack to Save Energy in MPI Programs

19th International Workshop, PATMOS 2009, Delft, The Netherlands, September 9-11, 2009, Revised Selected Papers

Impact of Dynamic Voltage Scaling (DVS) on Circuit Optimization

Recent Progress in the Boolean Domain

Approaches and Designs of Dynamic Voltage and Frequency Scaling

Dynamic Voltage/frequency Scaling and Power-gating of Network-on-chip with Machine Learning
Self-tuning Dynamic Voltage Scaling Techniques for Processor Design
Adaptive Digital Circuits for Power-Performance Range beyond Wide Voltage Scaling
Impact of Dynamic Voltage Scaling on Nano-Scale Circuit Optimization
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Investigating Fine-grained Voltage Scaling
Architectures for Low Power Signal Processing Applications
Tackling Energy Efficiency at Large Scale

Dynamic Voltage Scaling And Power Management For Portable
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edited by

KENDRA JOVANY

Controlling Energy Demand in Mobile Computing Systems
Springer Science & Business Media

The book provides a comprehensive coverage of different aspects of low power circuit synthesis at various levels of design hierarchy; starting from the layout level to the system level. For a seamless understanding of the subject, basics of MOS circuits has been introduced at transistor, gate and circuit level; followed by various low-power design methodologies, such as supply voltage

scaling, switched capacitance minimization techniques and leakage power minimization approaches. The content of this book will prove useful to students, researchers, as well as practicing engineers.

Dynamic Voltage Scaling with Feedback Scheduling for Real-time Embedded Systems

Springer
In the last few years, power dissipation has become an important design constraint, on par with performance, in the design of new computer systems. Whereas in the past, the primary job of the computer architect was to translate improvements in operating frequency and transistor count into performance, now power efficiency must be taken into account at every step of the design process. While for some time, architects have been successful in delivering 40% to 50% annual improvement in processor performance, costs that were previously brushed aside eventually caught up. The most critical of these costs is the inexorable increase in power dissipation and power density in processors. Power dissipation issues have catalyzed new topic areas in computer architecture, resulting in a

substantial body of work on more power-efficient architectures. Power dissipation coupled with diminishing performance gains, was also the main cause for the switch from single-core to multi-core architectures and a slowdown in frequency increase. This book aims to document some of the most important architectural techniques that were invented, proposed, and applied to reduce both dynamic power and static power dissipation in processors and memory hierarchies. A significant number of techniques have been proposed for a wide range of situations and this book synthesizes those techniques by focusing on their common characteristics . Table of Contents: Introduction / Modeling, Simulation, and Measurement / Using Voltage and Frequency Adjustments to Manage Dynamic Power / Optimizing Capacitance and Switching Activity to Reduce Dynamic Power / Managing Static (Leakage) Power / Conclusions

Multi-voltage CMOS Circuit Design

Springer Science & Business Media

This book presents an in-depth treatment of various power reduction and speed enhancement

techniques based on multiple supply and threshold voltages. A detailed discussion of the sources of power consumption in CMOS circuits will be provided whilst focusing primarily on identifying the mechanisms by which sub-threshold and gate oxide leakage currents are generated. The authors present a comprehensive review of state-of-the-art dynamic, static supply and threshold voltage scaling techniques and discuss the pros and cons of supply and threshold voltage scaling techniques.

Power Aware Computing

Cambridge Scholars Publishing

Dynamic voltage scaling (DVS) is a promising method to reduce the power consumption of CMOS-based embedded processors. However, pure DVS techniques do not perform well for dynamic systems where the execution times of different jobs vary significantly. A novel DVS scheme with feedback control mechanisms for hard real-time systems is proposed in this work. It produces energy-efficient schedules for both static and dynamic workloads. Task-splitting, slack-passing and preemption-handling schemes are proposed to

aggressively reduce the speed of each task. Different feedback control structures are integrated into the DVS algorithm to make it adaptable to workload variations. This scheme relies strictly on operating system support. It is evaluated in simulation as well as on an embedded platform. For given task sets, simulation experiments demonstrate the benefits of this scheme with savings of up to 29\% in energy over previous work. This scheme exhibits up to 24\% additional energy savings over other DVS algorithms on the embedded platform. The feedback-based DVS scheme is further extended to be leakage aware, which considers not only dynamic but also static power consumption caused by leakage current in circuits. A combined DVS, delay and sleeping scheme is proposed for architectures where static power exceeds dynamic power in some cases. DVS is used when dynamic power dominates the total power consumption, while a sleep mode is entered when static power becomes dominant. The extended algorithm, DVSleak, shows 30\% additional energy savings on average over a pure DVS algorithm in the simulation

experiment. Low-Power VLSI Circuits and Systems Power Switch Characterization for Fine-grained Dynamic Voltage Scaling200-MHz Digital Low-dropout Regulator with Dynamic Voltage Scaling for Power ManagementApproaches and Designs of Dynamic Voltage and Frequency ScalingDynamic Voltage Scaling Techniques for Power-efficient MPEG DecodingImpact of Dynamic Voltage Scaling on Nano-Scale Circuit Optimization45-nm CMOS Technology This book offers the first comprehensive coverage of digital design techniques to expand the power-performance tradeoff well beyond that allowed by conventional wide voltage scaling. Compared to conventional fixed designs, the approach described in this book makes digital circuits more versatile and adaptive, allowing simultaneous optimization at both ends of the power-performance spectrum. Drop-in solutions for fully automated and low-effort design based on commercial CAD tools are discussed extensively for processors, accelerators and on-chip memories, and are applicable to prominent applications (e.g., IoT, AI, wearables, biomedical). Through the higher power-performance versatility

techniques described in this book, readers are enabled to reduce the design effort through reuse of the same digital design instance, across a wide range of applications. All concepts the authors discuss are demonstrated by dedicated testchip designs and experimental results. To make the results immediately usable by the reader, all the scripts necessary to create automated design flows based on commercial tools are provided and explained. Springer Science & Business Media "Previously, research and design of Network-on-Chip (NoC) paradigms where mainly focused on improving the performance of the interconnectio n networks. With emerging wide range of low-power applications and energy constrained high-performance applications, it is highly desirable to have NoCs that are highly energy efficient without incurring performance penalty. In the design of high-performance massive multi-core chips, power and heat have become dominant constrains. Increased power consumption can raise chip temperature, which in turn can decrease chip reliability and performance and increase cooling costs.

It was proven that Small-world Wireless Network-on-Chip (SWNoC) architecture which replaces multi-hop wire-line path in a NoC by high-bandwidth single hop long range wireless links, reduces the overall energy dissipation when compared to wire-line mesh-based NoC architecture. However, the overall energy dissipation of the wireless NoC is still dominated by wire-line links and switches (buffers). Dynamic Voltage Scaling is an efficient technique for significant power savings in microprocessors. It has been proposed and deployed in modern microprocessors by exploiting the variance in processor utilization. On a Network-on-Chip paradigm, it is more likely that the wire-line links and buffers are not always fully utilized even for different applications. Hence, by exploiting these characteristics of the links and buffers over different traffic, DVFS technique can be incorporated on these switches and wire-line links for huge power savings. In this thesis, a history based DVFS mechanism is proposed. This mechanism uses the past utilization of the wire-line links & buffers to predict the future traffic and accordingly tune the

voltage and frequency for the links and buffers dynamically for each time window. This mechanism dynamically minimizes the power consumption while substantially maintaining a high performance over the system. Performance analysis on these DVFS enabled Wireless NoC shows that, the overall energy dissipation is improved by around 40% when compared

Small-world Wireless NoCs."--Abstract. Integrated Circuit and System Design: Power and Timing Modeling, Optimization and Simulation Springer Science & Business Media Energy consumption has become a primary concern in the last decade. One highly effective way to reduce CPU energy while still executing applications is dynamic voltage scaling (DVS).

While DVS makes runtime transitions between power levels possible, thus far the scheduling of DVS has only been implemented at the system levels. The primary reason for this is that a transition has significant time and energy costs and therefore must be restricted. On the other hand, if developers are given control over DVS and the flexibility to apply it as

necessary, then DVS scheduling decisions can include application-specific knowledge. We have developed a runtime support module for developer-driven dynamic voltage scaling (D3VS). The module allows applications to be densely populated with DVS scale requests, yet restricts the DVS overhead to 4% under reasonable assumptions. To do this, the module does not make power level transitions at every request. Instead, using the past history as hints, it picks a single power level that is representative of the application's behavior. In this thesis we present the analytical models and simulations used in the design of the D3VS runtime support module.

Just-in-Time Dynamic Voltage Scaling:

Exploiting Inter-Node Slack to Save Energy in MPI Programs

Springer Science & Business Media Circuit designers perform optimization procedures targeting speed and power. Gate sizing can be applied to optimize for speed, while Dual-VT and Dynamic Voltage Scaling (DVS) can be applied to optimize for leakage and

dynamic power, respectively. Both gate sizing and Dual-VT are design-time techniques applied to the circuit at a fixed voltage. DVS is a run-time technique and implies that the circuit will be operating at a different voltage than that used during optimization at design-time. After some analysis, the risk of non-critical paths becoming critical paths at run-time is detected under these circumstances. The following questions arise: 1) should we take DVS into account during optimization? 2) Does DVS impose any restrictions to design-time circuit optimizations? This is a case study of applying DVS to a circuit that has been optimized for speed and power, and aims at answering the previous two questions. We used a 45-nm CMOS design kit and flow for ISCAS'85 c432. Results showed that we should not optimize using Dual-VT at an arbitrary voltage but at the lowest in the DVS range, otherwise non-critical paths might become critical paths at run-time. 19th International Workshop, PATMOS 2009, Delft, The Netherlands, September 9-11, 2009, Revised Selected Papers LAP Lambert Academic Publishing In today’s world, people

are using more and more digital systems in daily life. Such systems utilize the elementariness of Boolean values. A Boolean variable can carry only two different Boolean values: FALSE or TRUE (0 or 1), and has the best interference resistance in technical systems. However, a Boolean function exponentially depends on the number of its variables. This exponential complexity is the cause of major problems in the process of design and realization of circuits. According to Moore's Law, the complexity of digital systems approximately doubles every 18 months. This requires comprehensive knowledge and techniques to solve very complex Boolean problems. This book summarizes the recent progress in the Boolean domain in solving such issues. Part 1 describes the most powerful approaches in solving exceptionally complex Boolean problems. It is shown how an extremely rare solution could be found in a gigantic search space of more than 10^195 (this is a number of 196 decimal digits) different color patterns. Part 2 describes new research into digital circuits that realize Boolean functions. This part contains

the chapters “Design” and “Test”, which present solutions to problems of power dissipation, and the testing of digital circuits using a special data structure, as well as further topics. Part 3 contributes to the scientific basis of future circuit technologies, investigating the need for completely new design methods for the atomic level of quantum computers. This section also concerns itself with circuit structures in reversible logic as the basis for quantum logic.

Impact of Dynamic Voltage Scaling (DVS) on Circuit Optimization

University-Press.org

Although users of high-performance computing are most interested in raw performance, both energy and power consumption have become critical concerns. As a result improving energy efficiency of nodes on HPC machines has become important and the importance of power-scalable clusters, where the frequency and voltage can be dynamically modified, has increased. This thesis investigates the energy consumption and execution time of applications on a power-scalable cluster. It studies intra-node and inter-node effects of memory and

communication bottlenecks. Results show that a power-scalable cluster has the potential to save energy by scaling the processor down to lower energy levels. This thesis presents a model that predicts the energy-time trade-off for larger clusters. On power-scalable clusters, one opportunity for saving energy with little or no loss of performance exists when the computational load is not perfectly balanced. This situation occurs frequently, as keeping the load balanced between nodes is one of the long standing fundamental problems in parallel and distributed computing. However, despite the large body of research aimed at balancing load both statically and dynamically, this problem is quite difficult to solve. This thesis presents a system called Jitter that reduces the frequency on nodes that are assigned less computation and therefore have idle time or slack time. This saves energy on these nodes, and the goal of Jitter is to attempt to ensure that they arrive 'just in time' so that they avoid increasing overall execution time. Specifically, we dynamically determine which nodes have enough slack time so that they can

be slowed down, which will greatly reduce the consumed energy on that node. Thus a superior energy-time trade-off can be achieved. This thesis studies a suite of MPI benchmarks, which are profiled, gathering information about the computation and communicatio n occuring in the application. This information is used to analyse various ene. **Recent Progress in the Boolean Domain** John Wiley & Sons System-Level Design Techniques for Energy-Efficient Embedded Systems addresses the development and validation of co-synthesis techniques that allow an effective design of embedded systems with low energy dissipation. The book provides an overview of a system-level co-design flow, illustrating through examples how system performance is influenced at various steps of the flow including allocation, mapping, and scheduling. The book places special emphasis upon system-level co-synthesis techniques for architectures that contain voltage scalable processors, which can dynamically trade off between computational performance and power consumption. Throughout the book, the

introduced co-synthesis techniques, which target both single-mode systems and emerging multi-mode applications, are applied to numerous benchmarks and real-life examples including a realistic smart phone.

Approaches and Designs of Dynamic Voltage and Frequency Scaling

Morgan & Claypool Publishers

Network-on-chip (NoC) continues to be the preferred communicatio n fabric in multicore and manycore architectures as the NoC seamlessly blends the resource efficiency of the bus with the parallelization of the crossbar. However, without adaptable power management the NoC suffers from excessive static power consumption at higher core counts. Static power consumption will increase proportionally as the size of the NoC increases to accommodate higher core counts in the future. NoC also suffers from excessive dynamic energy as traffic loads fluctuate throughout the execution of an application. Power-gating (PG) and Dynamic Voltage and Frequency Scaling (DVFS) are two highly effective techniques proposed in literature to reduce static power and dynamic energy in the NoC

respectively. DVFS is a popular technique that allows dynamic energy to be saved but may potentially lead to a loss in throughput. Power-gating allows static power to be saved but can introduce new problems incurred by isolating network routers.

Dynamic Voltage/frequency Scaling and Power-gating of Network-on-chip with Machine Learning

Morgan & Claypool Publishers Managing the power consumption of circuits and systems is now considered one of the most important challenges for the semiconductor industry. Elaborate power management strategies, such as dynamic voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This book explores existing

solutions for power-aware test and design-for-test of conventional circuits and systems, and surveys test strategies and EDA solutions for testing low power devices.

Self-tuning Dynamic Voltage Scaling Techniques for Processor Design

Springer

Welcome to the proceedings of the 19th International Workshop on Power and TimingModeling, Optimizationa ndSimulation, PATMOS2009. Overtheyears, PATMOShasevolvedintoanimportantEuropeanevent, whereresearchersfrom both industry and academia discuss and investigate the emerging challenges in future and contemporary applications, design methodologies, and tools required for the development of the upcoming generations of integrated circuits and s-tems. PATMOS 2009 was organized by TU Delft, The Netherlands, with sp-sorship by the NIRICT Design Lab and Cadence Design Systems, and technical co-sponsorshipby theIEEE.Furtherinformationaboutttheworkshopisavailable athttp://ens.ewi.tudelft.nl/patmos09. The technical programof PATMOS 2009 contained state-of-the-arttechnical contributions, three invited keynotes, and a special session on SystemC-AMS Extensions.

The technical program focused on timing, performance, and power consumption, as well as architectural aspects with particular emphasis on m- eling, design, characterizati on, analysis, and optimization in the nanometer era. The Technical Program Committee, with the assistance of additional expert reviewers, selected the 36 papers presented at PATMOS. The papers were - ganized into 7 oral sessions (with a total of 26 papers) and 2 poster sessions (with a total of 10 papers). As is customary for the PATMOS workshops, full papers were required for review, and a minimum of three reviews were received per manuscript. Adaptive Digital Circuits for Power-Performance Range beyond Wide Voltage Scaling CRC Press Power Switch Characterizati on for Fine-grained Dynamic Voltage Scaling200-MHz Digital Low-dropout Regulator with Dynamic Voltage Scaling for Power ManagementA pproaches and Designs of Dynamic Voltage and Frequency ScalingDynam ic Voltage Scaling Techniques for Power-efficient MPEG DecodingImpa ct of Dynamic Voltage Scaling on Nano-Scale Circuit Optimization4 5-nm CMOS

TechnologyLAP Lambert Academic Publishing

Impact of Dynamic Voltage Scaling on Nano-Scale Circuit Optimization

Springer Nature
This thesis investigates Dynamic Voltage Scaling (DVS) techniques to lower power consumption in video decoding. A DVS scheme called the Frame-data Computation Aware (FDCA) method has been presented. This method is adaptable not only to stored video applications but also to real-time video scenarios. Unlike DVS schemes for video decoding proposed earlier, the FDCA scheme does not require any preprocessing mechanisms. Results from simulations performed using the scheme are presented and compared with prior existing DVS schemes. The results indicate that the FDCA method provides power saving of up to an average of about 68%.

Compiler-directed Dynamic Voltage and Frequency Scaling for CPU Power and Energy Reduction

Springer Science & Business Media
Keywords: dynamic voltage scaling, energy-time trade-off, load-imbalance, MPI.

Investigating Fine-grained Voltage Scaling Architectures for Low Power Signal Processing Applications

Circuit designers perform optimization procedures targeting speed and power during the design of a circuit. Gate sizing can be applied to optimize for speed, while Dual-VT and Dynamic Voltage Scaling (DVS) can be applied to optimize for leakage and dynamic power, respectively. Both gate sizing and Dual-VT are design-time techniques, which are applied to the circuit at a fixed voltage. On the other hand, DVS is a run-time technique and implies that the circuit will be operating at a different voltage than that used during the optimization phase at design-time. After some analysis, the risk of non-critical paths becoming critical paths at run-time is detected under these circumstances. The following questions arise: 1) should we take DVS into account during the optimization phase? 2) Does DVS impose any restrictions while performing design-time circuit optimizations? This thesis is a case study of applying DVS to a circuit that has been optimized for speed and power, and aims at answering the previous two questions. We used a 45-nm

CMOS design kit and flow. Synthesis, placement and routing, and timing analysis were applied to the benchmark circuit ISCAS'85 c432. Logical Effort and Dual-VT algorithms were implemented and applied to the circuit to optimize for speed and leakage power, respectively. Optimizations were run for the circuit operating at different voltages. Finally, the impact of DVS on circuit optimization was studied based on HSPICE simulations sweeping the supply voltage for each optimization. The results showed that DVS had no impact on gate sizing optimizations, but it did on Dual-VT optimizations. It is shown that we should not optimize at an arbitrary voltage. Moreover, simulations showed that Dual-VT optimizations should be performed at the lowest voltage that DVS is intended to operate, otherwise non-critical paths will become critical paths at run-time.

Tackling Energy Efficiency at Large Scale

State-of-the-Art Approaches to Advance the Large-Scale Green Computing Movement Edited by one of the founders and lead investigator of the Green500 list, The Green Computing Book: Tackling Energy

Efficiency at Large Scale explores seminal research in large-scale green computing. It begins with low-level, hardware-based approaches and then traverses up the software stack with increasingly higher-level, software-based approaches. In the first chapter, the IBM Blue Gene team illustrates how to improve the energy efficiency of a supercomputer by an order of magnitude without any system performance loss in parallelizable applications. The next few chapters explain how to enhance the energy efficiency of a large-scale computing system via compiler-directed energy optimizations, an adaptive run-time system, and a general prediction performance framework. The book then explores the interactions between energy management and reliability and describes storage system organization that maximizes energy efficiency and reliability. It also addresses the need for coordinated power control across different layers and covers demand response policies in computing centers. The final chapter assesses the impact of servers on data center costs.

Power Optimizations

for the MLCA Using Dynamic Voltage Scaling Power Aware Design Methodologies was conceived as an effort to bring all aspects of power-aware design methodologies together in a single document. It covers several layers of the design hierarchy from technology, circuit logic, and architectural levels up to the system layer. It includes discussion of techniques and methodologies for improving the power efficiency of CMOS circuits (digital and analog), systems on chip, microelectronic systems, wirelessly networked systems of computational nodes and so on. In addition to providing an in-depth analysis of the sources of power dissipation in VLSI circuits and systems and the technology and design trends, this book provides a myriad of state-of-the-art approaches to power optimization and control. The different chapters of Power Aware Design Methodologies have been written by leading researchers and experts in their respective areas. Contributions are from both academia and industry. The contributors have reported the various technologies, methodologies, and techniques in such a way that they are

understandabl e and useful.

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