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Analysis Of Low Power And Area Efficient Cmos Comparator

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Statistical Power Analysis
2017 Innovations in Power and Advanced Computing Technologies (i-PACT)
Low-Power Variation-Tolerant Design in Nanometer Silicon
Soft Computing and Signal Processing
Low Power Design in Deep Submicron Electronics
High-Level Power Analysis and Optimization
Design and Analysis of Low-power High-speed Shared Charge Reset Technique Based Dynamic Latch Comparator
Practical Low Power Digital VLSI Design
Analysis and Damping Control of Power System Low-frequency Oscillations
Design of Low Power Integrated Radios for Emerging Standards
The Design of Low-Voltage, Low-Power Sigma-Delta Modulators
Handbook of Research on Emerging Technologies for Electrical Power Planning, Analysis, and Optimization

Nanoelectronics, Circuits and Communication Systems
Design and Analysis of Low-power and Noise-tolerant Multiply Accumulate Units
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Design and Analysis of Low-power SRAMs
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Design for High Performance, Low Power, and Reliable 3D Integrated Circuits
Security and Privacy-Preserving Techniques in Wireless Robotics
Introduction to Power Analysis
Mixed Analog-digital VLSI Devices and Technology

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Statistical Power Analysis

John Wiley & Sons
You are responsible for planning and designing electrical power systems? Good. Hopefully you know your way through national and international regulations, safety standards, and all the possible pitfalls you will encounter. You're not sure? This volume provides you with the wealth of experience the author gained in 20 years of practice. The enclosed CAD software accelerates your planning process and makes your final design cost-efficient and secure.
2017 Innovations in Power and Advanced Computing Technologies (i-PACT)
Springer
CD-ROM contains: "easy-to-use statistical power analysis program."

Low-Power Variation-Tolerant Design in Nanometer Silicon

An ASIC Low Power Primer
Statistical Power Analysis explains the key concepts in statistical power analysis and illustrates their application in both tests of traditional null hypotheses (that treatments or interventions have no effect in the population) and in tests of the minimum-effect hypotheses (that the population effects of treatments or interventions are so small that they can be safely treated as unimportant). It provides readers with the tools to understand and perform power analyses for virtually all the statistical methods used in the social and behavioral sciences. Brett Myors and Kevin Murphy apply the latest approaches of power analysis to both null hypothesis and minimum-effect testing using the same basic unified model. This book starts with a review of the key concepts that underly statistical power. It goes on to show how to perform and interpret power analyses, and the ways to use them to diagnose and plan research. We discuss the uses of power analysis in correlation and regression, in the analysis of experimental data, and in multilevel studies. This edition includes new material and new power software. The programs used for power analysis in this book have been re-written in R, a language that is widely used and freely available. The authors include R codes for all programs, and we have also provided a web-based app that allows users who are not comfortable with R to perform a wide range of analyses using any computer or device that provides access to the web. Statistical Power Analysis helps readers design studies, diagnose existing studies, and understand why hypothesis tests come out the way they do. The fifth edition

includes updates to all chapters to accommodate the most current scholarship, as well as recalculations of all examples. This book is intended for graduate students and faculty in the behavioral and social sciences; researchers in other fields will find the concepts and methods laid out here valuable and applicable to studies in many domains.

Soft Computing and Signal Processing Springer Science & Business Media

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Low Power Design in Deep Submicron Electronics CRC Press

This book describes novel and disruptive architecture and circuit design techniques, toward the realization of low-power, standard-compliant radio architectures and silicon implementation of the circuits required for a variety of leading-edge applications. Readers will gain an understanding of the circuit level challenges that exist for low power radios, compatible with the IEEE 802.15.6 standard. The authors discuss current techniques to address some of these challenges, helping readers to understand the state-of-the-art, and to address the various, open research problems that exist with respect to realizing low power radios. Enables readers to face challenging bottleneck in low power radio design, with state-of-the-art, circuit-level design techniques; Provides readers with basic knowledge of circuits suitable for low power radio circuits compatible with the IEEE 802.15.6 standard; Discusses new and emerging architectures and circuit techniques, enabling applications such as body area networks and internet of things.

High-Level Power Analysis and Optimization Springer Science & Business Media

The explosive growth of battery operated devices has made low-power design a priority in recent years. Moreover, embedded SRAM units have become an important block in modern SoCs. The increasing number of transistor count in the SRAM units and the surging leakage current of the MOS transistors in the scaled technologies have made the SRAM unit a power hungry block from both dynamic and static perspectives. Owing to high bitline voltage swing during write operation, the write power consumption is dominated the dynamic power consumption. The static power consumption is mainly due to the leakage current associated with the SRAM cells distributed in the array. Moreover, as supply voltage decreases to tackle the power consumption, the data stability of the SRAM cells have become a major concern in recent years. To reduce the write power consumption, several schemes such as row based sense amplifying cell (SAC) and hierarchical bitline sense amplification (HBLSA) have been proposed. However, these schemes impose architectural limitations on the design in terms of the number of words on a row. Beside, the effectiveness of these methods is limited to the dynamic power consumption. Conventionally, reduction of the cell supply voltage and exploiting the body effect has been suggested to reduce the cell leakage current. However, variation of the supply voltage of the cell associates with a higher dynamic power consumption and reduced cell data stability. Conventionally qualified by Static Noise Margin (SNM), the ability of the cell to retain the data is reduced under a lower supply voltage conditions. In this thesis, we revisit the concept of data stability from the dynamic

perspective. A new criteria for the data stability of the SRAM cell is defined. The new criteria suggests that the access time and non-access time (recovery time) of the cell can influence the data stability in a SRAM cell. The speed vs. stability trade-off opens new opportunities for aggressive power reduction for low-power applications. Experimental results of a test chip implemented in a 130 nm CMOS technology confirmed the concept and opened a ground for introduction of a new operational mode for the SRAM cells. We introduced a new architecture; Segmented Virtual Grounding (SVGND) to reduce the dynamic and static power reduction in SRAM units at the same time. Thanks to the new concept for the data stability in SRAM cells, we introduced the new operational mode of Accessed Retention Mode (AR-Mode) to the SRAM cell. In this mode, the accessed SRAM cell can retain the data, however, it does not discharge the bitline. The new architecture outperforms the recently reported low-power schemes in terms of dynamic power consumption, thanks to the exclusive discharge of the bitline and the cell virtual ground. In addition, the architecture reduces the leakage current significantly since it uses the back body biasing in both load and drive transistors. A 40Kb SRAM unit based on SVGND architecture is implemented in a 130 nm CMOS technology. Experimental results exhibit a remarkable static and dynamic power reduction compared to the conventional and previously reported low-power schemes as expect from the simulation results.

Design and Analysis of Low-power High-speed Shared Charge Reset Technique Based Dynamic Latch Comparator CRC Press

Power consumption is a key limitation in many high-speed and high-data-rate electronic systems today, ranging from mobile telecom to portable and desktop computing systems, especially when moving to nanometer technologies. Ultra Low-Power Electronics and Design offers to the reader the unique opportunity of accessing in an easy and integrated fashion a mix of tutorial material and advanced research results, contributed by leading scientists from academia and industry, covering the most hot and up-to-date issues in the field of the design of ultra low-power devices, systems and applications.

Practical Low Power Digital VLSI Design Taylor & Francis

This book presents the cross-layer design and optimization of wake-up receivers for wireless body area networks (WBAN), with an emphasis on low-power circuit design. This includes the analysis of medium access control (MAC) protocols, mixer-first receiver design, and implications of receiver impairments on wideband frequency-shift-keying (FSK) receivers. Readers will learn how the overall power consumption is reduced by exploiting the characteristics of body area networks. Theoretical models presented are validated with two different receiver implementations, in 90nm and 40nm CMOS technology.

Analysis and Damping Control of Power System Low-frequency Oscillations Springer Nature

This book presents the research and development results on power systems oscillations in three categories of analytical methods. First is damping torque analysis which was proposed in 1960’s, further developed between 1980-1990, and widely used in industry. Second is modal analysis which

developed between the 1980's and 1990's as the most powerful method. Finally the linearized equal-area criterion analysis that is proposed and developed recently. The book covers three main types of controllers: Power System Stabilizer (PSS), FACTS (Flexible AC Transmission Systems) stabilizer, and ESS (Energy Storage Systems) stabilizer. The book provides a systematic and detailed introduction on the subject as the reference for industry applications and academic research.

Design of Low Power Integrated Radios for Emerging Standards Springer Science & Business Media

Practical Low Power Digital VLSI Design emphasizes the optimization and trade-off techniques that involve power dissipation, in the hope that the readers are better prepared the next time they are presented with a low power design problem. The book highlights the basic principles, methodologies and techniques that are common to most CMOS digital designs. The advantages and disadvantages of a particular low power technique are discussed. Besides the classical area-performance trade-off, the impact to design cycle time, complexity, risk, testability and reusability are discussed. The wide impacts to all aspects of design are what make low power problems challenging and interesting. Heavy emphasis is given to top-down structured design style, with occasional coverage in the semicustom design methodology. The examples and design techniques cited have been known to be applied to production scale designs or laboratory settings. The goal of Practical Low Power Digital VLSI Design is to permit the readers to practice the low power techniques using current generation design style and process technology. Practical Low Power Digital VLSI Design considers a wide range of design abstraction levels spanning circuit, logic, architecture and system. Substantial basic knowledge is provided for qualitative and quantitative analysis at the different design abstraction levels. Low power techniques are presented at the circuit, logic, architecture and system levels. Special techniques that are specific to some key areas of digital chip design are discussed as well as some of the low power techniques that are just appearing on the horizon. Practical Low Power Digital VLSI Design will be of benefit to VLSI design engineers and students who have a fundamental knowledge of CMOS digital design.

The Design of Low-Voltage, Low-Power Sigma-Delta Modulators Springer Science & Business Media

Power Aware Design Methodologies was conceived as an effort to bring all aspects of power-aware design methodologies together in a single document. It covers several layers of the design hierarchy from technology, circuit logic, and architectural levels up to the system layer. It includes discussion of techniques and methodologies for improving the power efficiency of CMOS circuits (digital and analog), systems on chip, microelectronic systems, wirelessly networked systems of computational nodes and so on. In addition to providing an in-depth analysis of the sources of power dissipation in VLSI circuits and systems and the technology and design trends, this book provides a myriad of state-of-the-art approaches to power optimization and control. The different chapters of Power Aware Design Methodologies have been written by leading researchers and experts in their respective areas. Contributions are from both academia and industry. The

contributors have reported the various technologies, methodologies, and techniques in such a way that they are understandable and useful.

Handbook of Research on Emerging Technologies for Electrical Power Planning, Analysis, and Optimization Routledge

The power consumption of integrated circuits is one of the most problematic considerations affecting the design of high-performance chips and portable devices. The study of power-saving design methodologies now must also include subjects such as systems on chips, embedded software, and the future of microelectronics. Low-Power Electronics Design covers all major aspects of low-power design of ICs in deep submicron technologies and addresses emerging topics related to future design. This volume explores, in individual chapters written by expert authors, the many low-power techniques born during the past decade. It also discusses the many different domains and disciplines that impact power consumption, including processors, complex circuits, software, CAD tools, and energy sources and management. The authors delve into what many specialists predict about the future by presenting techniques that are promising but are not yet reality. They investigate nanotechnologies, optical circuits, ad hoc networks, e-textiles, as well as human powered sources of energy. Low-Power Electronics Design delivers a complete picture of today's methods for reducing power, and also illustrates the advances in chip design that may be commonplace 10 or 15 years from now.

Nanoelectronics, Circuits and Communication Systems Springer Science & Business Media

High-Level Power Analysis and Optimization presents a comprehensive description of power analysis and optimization techniques at the higher (architecture and behavior) levels of the design hierarchy, which are often the levels that yield the most power savings. This book describes power estimation and optimization techniques for use during high-level (behavioral synthesis), as well as for designs expressed at the register-transfer or architecture level. High-Level Power Analysis and Optimization surveys the state-of-the-art research on the following topics: power estimation/macromodeling techniques for architecture-level designs, high-level power management techniques, and high-level synthesis optimizations for low power. High-Level Power Analysis and Optimization will be very useful reading for students, researchers, designers, design methodology developers, and EDA tool developers who are interested in low-power VLSI design or high-level design methodologies.

Design and Analysis of Low-power and Noise-tolerant Multiply Accumulate Units Springer Science & Business Media

Design considerations for low-power operations and robustness with respect to variations typically impose contradictory requirements. Low-power design techniques such as voltage scaling, dual-threshold assignment and gate sizing can have large negative impact on parametric yield under process variations. This book focuses on circuit/architectural design techniques for achieving low power operation under parameter variations. We consider both logic and memory design aspects and cover modeling and analysis, as well as design methodology to achieve simultaneously low power and variation tolerance, while minimizing design

overhead. This book will discuss current industrial practices and emerging challenges at future technology nodes.
Particle Analysis by Low Power He-Ne Laser Springer Science & Business Media
The wide gap between the existing security solutions and the actual practical deployment in smart manufacturing, smart home, and remote environments (with respect to wireless robotics) is one of the major reasons why we require novel strategies, mechanisms, architectures, and frameworks. Furthermore, it is also important to access and understand the different level of vulnerabilities and attack vectors in Wireless Sensor Network (WSN) and Wireless Robotics. This book includes an in-depth explanation of a secure and dependable Wireless Robotics (WR) architecture, to ensure confidentiality, authenticity, and availability. Features Blockchain technology for securing data at end/server side Emerging technologies/networking, like Cloud, Edge, Fog, etc., for communicating and storing data (securely). Various open issues, challenges faced in this era towards wireless robotics, including several future research directions for the future. Several real world's case studies are included Chapters on ethical concerns and privacy laws, i.e., laws for service providers Security and privacy challenges in wireless sensor networks and wireless robotics The book is especially useful for academic researchers, undergraduate students, postgraduate students, and industry researchers and professionals.
Design and Analysis of Low-power SRAMs Springer Science & Business Media
Improve your circuit-design potential with this expert guide to the devices and technology used in mixed analog-digital VLSI chips for such high-volume applications as hard-disk drives, wireless telephones, and consumer electronics. The book provides you with a critical understanding of device models, fabrication technology, and layout as they apply to mixed analog-digital circuits.You will learn about the many device-modeling requirements for analog work, as well as the pitfalls in models used today for computer simulators such as Spice. Also included is information on fabrication technologies developed specifically for mixed-signal VLSI chips, plus guidance on the layout of mixed analog-digital chips for a high degree of analog-device matching and minimum digital-to-analog interference.This reference book features an intuitive introduction to MOSFET operation that will enable you to view with insight any MOSFET model ? besides thorough discussions on valuable large-signal and small-signal models.Filled with practical information, this first-of-its-kind book will help you grasp the nuances of mixed-signal VLSI-device models and layout that are crucial to the design of high-performance chips.

Power Aware Design Methodologies

CRC Press
As the demand for efficient energy sources continues to grow around the globe, electrical systems are becoming more essential in an effort to meet these increased needs. As these systems are being utilized more frequently, it becomes imperative to find ways of optimizing their overall function. The Handbook of Research on Emerging Technologies for Electrical Power Planning, Analysis, and Optimization features emergent methods and

research in the systemic and strategic planning of energy usage. Highlighting theoretical perspectives and empirical research, this handbook is a comprehensive reference source for researchers, practitioners, students, and professionals interested in the current advancements and efficient use in power systems.

Design for High Performance, Low Power, and Reliable 3D Integrated Circuits

World Scientific
I PACT 2017 intends to provide a platform for the exchange of ideas amongst researchers, professionals, academicians, corporate & industry professionals, technically sound students and entrepreneurs in various disciplines across the globe to present the state of the art innovations in power and advanced computing technologies and point out the new trends in current research activities and emerging technologies.

Security and Privacy-Preserving Techniques in Wireless Robotics IGI Global
The book presents selected research papers on current developments in the field of soft computing and signal processing from the International Conference on Soft Computing and Signal Processing (ICSCSP 2018). It includes papers on current topics such as soft sets, rough sets, fuzzy logic, neural networks, genetic algorithms and machine learning, discussing various aspects of these topics, like technological, product implementation, contemporary research as well as application issues.

Introduction to Power Analysis Springer Science & Business Media
This book provides readers with a variety of algorithms and software tools, dedicated to the physical design of through-silicon-via (TSV) based, three-dimensional integrated circuits. It describes numerous “manufacturing-ready” GDSII-level layouts of TSV-based 3D ICs developed with the tools covered in the book. This book will also feature sign-off level analysis of timing, power, signal integrity, and thermal analysis for 3D IC designs. Full details of the related algorithms will be provided so that the readers will be able not only to grasp the core mechanics of the physical design tools, but also to be able to reproduce and improve upon the results themselves. This book will also offer various design-for-manufacturability (DFM), design-for-reliability (DFR), and design-for-testability (DFT) techniques that are considered critical to the physical design process.

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