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# Axi Reference Guide Xilinx

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MATLAB as AXI Master with Xilinx FPGA and Zynq SoC Boards ZYNQ AXI Interfaces  
Part 1 (Lesson 3) Developing application software for Xilinx AXI DMA Using AXI DMA  
in Vivado Generating custom AXI4-Stream IP core using Xilinx Vivado Blastoff!  
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Tutorial: Creating a simple AXI Slave Adder and interfacing with the Zynq FPGA SoC  
Zynq 7000 (lesson 10): AXI DMA in Direct Register Mode AXI Stream basics for  
beginners! A Stream FIFO example in Verilog. ZYNQ Training - session 09 - part IV -  
Transfer Data from PL to PS using AXI DMA Creating Custom AXI Master Interfaces  
Part 4 (Lesson 7) AXI Memory Mapped Interfaces Hardware Debugging in

Vivado (Lesson 5) Creating a custom AXI-Streaming IP in Vivado AXI Introduction Part 1: How AXI works and AXI-Lite transaction example Expanding Zynq with AXI BRAM and SPI Programmable Logic

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~~ZYNQ AXI Interfaces Part 1 (Lesson 3) Developing application software for Xilinx AXI~~

~~DMA Creating Custom IP on VHDL in VIVADO Design Suit for ZedBoard~~ **Creating Custom PYNQ Overlay with VIVADO HLS, IPI and Jupyter** Introduction to Direct Memory Access (DMA)

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Vivado PS Configuration Wizard Overview **ZYNQ Training - Session 04 - Designing with AXI using Xilinx Vivado Building Accelerated Applications with Vitis AXI Memory Mapped Interfaces \u0026amp; Hardware Debugging in Vivado (Lesson 5)** ~~FPGA Plug-and-Play Design with the AXI-4 Common Interconnect~~

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**- What Is An FPGA?** Polling/Interrupt/DMA differences explained easily **ZYNQ**  
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*Part 1: Vivado design Getting started with Vivado High Level Synthesis* Xilinx HLS #2: FPGA FIR Filter Design in C in 30 minutes (Vivado High Level Synthesis) *Dynamic Function Exchange with ZYNQ Ultrascale+ : Part 1: Introduction* ~~SDRA2020-03/04- Laurence Barker: Using Xilinx Vivado for SDR Development~~ **Video Interfacing with Zynq (FPGAs): Part 2 Using Xilinx AXI4 Stream to Video IP Using Xilinx IP Cores Within Your Design** ~~Using Vivado Serial IO Analyzer~~ **Xilinx SDK System Performance Tools Overview**

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Interfaces Part 1 (Lesson 3) Developing  
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Creating Custom IP on VHDL in VIVADO

Design Suit for ZedBoard **Creating  
Custom PYNQ Overlay with VIVADO  
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Vivado PS Configuration Wizard  
Overview **ZYNQ Training - Session 04  
- Designing with AXI using Xilinx  
Vivado Building Accelerated**

## Applications with Vitis AXI Memory Mapped Interfaces \u0026amp; Hardware Debugging in Vivado (Lesson 5)

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- Write Address Channel
- Read Data Channel
- Write Data Channel
- Memory Access Channel

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 release: • Included description of  
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The Xilinx® AXI Hardware Internal Configuration Access Port (HWICAP) LogiCORE™ IP core for the AXI Interface enables an embedded microprocessor, such as the MicroBlaze™ processor, to read and write the FPGA configuration memory through the Internal Configuration Access Port (ICAPEn). *Xilinx AXI-Based IP Overview - Application Notes ...*

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DS759 March 1, 2011 www.xilinx.com 2  
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Access (DMA)~~

Vivado PS Configuration Wizard  
Overview **ZYNQ Training - Session 04  
- Designing with AXI using Xilinx  
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Applications with Vitis AXI Memory  
Mapped Interfaces \u0026amp; Hardware  
Debugging in Vivado (Lesson 5)**  
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 The recent adoption of the AXI4 by Xilinx for all of their current and future device families and products, including the Zynq™-7000 family of Extensible Processing Platform (EPP) products , makes this protocol vital to learn for every SoC designer in order to be able to use the newest device families from major silicon vendors, and access a wide

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- Updated Xilinx 04/06/2016 2016.1 Updated for Vivado 2016.1 release:
- Included description of address extension, new in version 9.6.
- Included description of pipeline pause functionality, new in version 9.6
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